

### Application Note 100

### February 2006

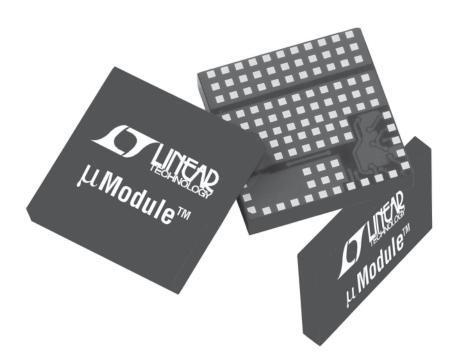
# Recommended Land Pad Design, Assembly and Rework Guidelines for DC/DC µModule in LGA Package

David Pruitt

#### **1.1 INTRODUCTION**

The Linear Technology  $\mu$ Module<sup>TM</sup> solution combines integrated circuits and passive components in a single package. The  $\mu$ Module integrates several technologies to bring a cost effective, advanced solution which maximizes board space and improves electrical and thermal performance. The  $\mu$ Module is overmolded in a solid array and individual units are saw singulated. All  $\mu$ Module components are leadless with electrical connections being made through the land pad array.

 $\mathcal{LT}$ , LTC and LTM are registered trademarks of Linear Technology Corporation.  $\mu$ Module is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.



#### **ARTICLE INDEX**

1.0	<b>Linear Technology LTM</b> μ <b>Module</b> 1.1 Introduction	1
2.0	Manufacturing Considerations 2.1 SMT Process	3
3.0	PCB Design Guidelines 3.1 Land Pad Styles 3.2 Land Pad Design 3.3 Design of PCB Land Pattern for Package Terminals 3.3.1 Thermal Pad Via Design 3.4 Surface Finishes	3 3 4
4.0	Solder Paste Screen Printing Process         4.1 Solder Paste         4.2 Solder Stencils         4.3 Pad Stencil Design	4
5.0	Package to Board Assembly Process         5.1 Placement and Alignment.         5.2 Solder Reflow         5.3 PCB Cleaning         5.4 Inspecting	5 6
6.0	Rework         6.1 PC Board Bake         6.2 PC Board Preheat         6.3 Reflow/Removal of the Component from the PCB         6.4 Cleaning and Prep of the PCB Land         6.5 Screen Printing of Solder Paste         6.6 Placement and Reflow of Component         6.7 Inspection of Reworked Solder Joints         6.8 Rework Equipment for µModule	7 7 7 7 7 7
7.0		
8.0	Appendix	8



#### 2.0 MANUFACTURING CONSIDERATIONS

#### 2.1 SMT Process

Many factors contribute to a high yielding PCB assembly process. A few of the key focus areas and their contributing factors are highlighted in Table 1.

#### **3.0 PCB DESIGN GUIDELINES**

One of the key efforts in implementing the  $\mu$ Module package on a PC board is the design of the land pattern. The  $\mu$ Module has square metallized pads exposed on the bottom surface of the package body. Electrical and mechanical connection between the component and the PC board is made by screen printing solder paste on the PC board and reflowing the paste after placement. To guarantee reliable solder joints it is essential to design the land pattern to the  $\mu$ Module pad pattern.

#### 3.1 Land Pad Styles/Solder Mask

The industry has debated the merits of solder mask defined (SMD) pads and non-solder mask defined (NSMD) pads (Copper defined), see Figure 1. Both styles are acceptable for use with the  $\mu$ Module package; the only limitation is the accuracy of the pads.

The tolerance of the  $\mu$ Module defines the method best used for your assembly process (see the LTM data sheet for drawing). The land pattern design for the  $\mu$ Module is SMD. The SMD is used due to the large current capabilities of the  $\mu$ Module.

For surface mounting of the  $\mu$ Module, NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than on solder masking. NSMD by

definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability.

#### 3.2 Land Pad Design

IPC is an industry organization with standard specifications for determining PCB land patterns. Since the  $\mu$ Module is a new package style, it is recommended that this application note be used in conjunction with evolving guidelines in IPC.

# 3.3 Design of PCB Land Pattern for Package Terminals

As a general rule, the PCB pad should be designed 0.00mm to 0.127mm larger than the package terminal pad. (Refer to the LTM data sheet drawing for recommended solder pad). Linear Technology recommends 0.20mm to 0.30mm extension of the solder pads as they exit away from the package body. This helps for solder inspection and also prevents solder balling.

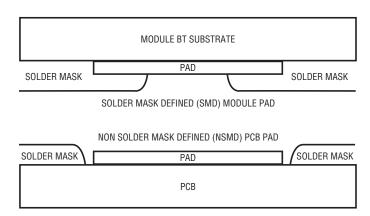


Figure 1. Module and PCB Pad Definition

Solder Paste Quality	Uniform Viscosity and Texture. Free from Foreign material. Solder Paste Should be Used Before the Expiration Date. Shipment and Storage Temperatures are Maintained within the specified range. Paste is Protected from Drying Out on the Solder Stencil.				
PCB Quality	Clean, Flat, Plated or Coated Solder Land Pad Area. Attachment Surface Must Be Clean and Free of Solder Mask Residue				
Placement Accuracy	Tight Tolerances Are Not Usually Required. LGA Packages Can Self-Center Themselves as Long as a Major Portion (More Than 50 Percent) of the Lead Finger Is in Contact with the Solder Paste Covered Land Area on the Board. Alignment Marks (Fiducials) on the PCB Are Helpful for Verifying Correct Placement of Parts				
Solder Reflow Profile	The Solder Reflow Will Be Dependent on PCB Design, PCB Thickness, Type of Components, Component Density, and the Recommended Profile of the Solder Paste Being Used. A Reflow Profile Will Need to be Developed for Each PCB Type Using Various LGA Packages. Refer to the Reflow Profile in the Solder Reflow Section (5.2)				

#### Table 1. General Guidelines for Assembly



#### 3.3.1 Thermal Pad Via Design

Thermal data  $(\theta_{JA})$  for the  $\mu$ Module is based on a 4-layer PCB incorporating vias, which act as the thermal path between the layers. Based on thermal performance requirements it is recommended to use a 4-layer PCB with filled vias to effectively remove heat from the device.

#### 3.4 Surface Finishes

There are a variety of surface finishes commonly available. The key factor in selecting an acceptable surface finish is to ensure that the land pads have a "uniform" surface. Irregular surface plating, uneven solder paste thickness or crowning of the solder plating can reduce overall surface mount yields. Bare Copper with an Organic Solderability Preservative (OSP) coating, electroless nickel/immersion gold or electroplated nickel/gold finishes have shown to provide an acceptable land pad surface. One type of surface finish that should be avoided is referred to as a dryfilm process. This is because the copper undercut can cause sidewall dewetting during the reflow process.

#### 4.0 SOLDER PASTE SCREEN PRINTING PROCESS

#### 4.1 Solder Paste

The quality of the paste print is an important factor in producing high yield assemblies. A Type 3 or 4, low residue, no-clean solder paste (Sn63/Pb37 or 95sn/3.5Ag/ 0.5Cu) is commonly used in mounting LGA packages, however water soluble flux materials are also widely used. Solder paste composition is often a compromise given the variety of components which must be placed on a PCB, and special SMT specific solder pastes are being marketed by solder paste vendors that minimize voiding in the solder joint (see section 5.2).

# 4.2 Solder Stencils (For More Detailed Information See Appendix A)

The formation of reliable solder joints is a necessity. The large numbers of pads on the  $\mu$ Module can present a challenge in producing an even solder line thickness. To this end, careful consideration must be applied to the stencil design. The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer

is critical for uniform reflow-solder processing. Stencils are usually made of brass or stainless steel, with stainless steel being more durable. Apertures should be trapezoidal to ensure uniform release of the solder paste and to reduce smearing. Hence dimension A < B. Refer to Figure 2.

The solder joint thickness for the  $\mu$ Module pad should be 50 $\mu$ m to 75 $\mu$ m after reflow. Thickness of the stencil (C) is usually in the 100 $\mu$ m to 150 $\mu$ m (.004" to .006") range. The actual thickness of a stencil is dependent on other surface mount devices on the PCB. A squeegee durometer of 95 or harder should be used. The blade angle, pressure, and speed must be fine-tuned to ensure even paste transfer. An inspection of the stenciled board is recommended before placing parts; as proper stencil application is the most important factor with regards to reflow yields later in the process. As a guide, it is recommended to use a stencil thickness of 125 $\mu$ m (.005") for the  $\mu$ Module.

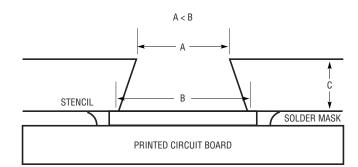


Figure 2. Cross Section View of  $\mu\text{Module}$  Stencil

#### 4.3 Pad Stencil Design

The pad opening stencil dimensions will depend on the specific  $\mu$ Module pad dimensions and the necessary aspect ratio. The aspect ratio relates to the manufacture of stencils. Stencil manufacturers will typically require the aspect ratios to be greater than 1.5. Reference IPC-7527.

ASPECT RATIO = Aperture Width/Stencil Thickness

#### **5.0 PACKAGE TO BOARD ASSEMBLY PROCESS**

#### 5.1 Placement and Alignment

The pick and place accuracy governs the package placement and rotational alignment. This is equipment/process dependent. Slightly misaligned parts (less than 50 percent off the pad center) will automatically self-align during reflow (see Figure 3). Grossly misaligned packages (greater





## Application Note 100

than 50 percent off pad center) should be removed prior to reflow as they may develop electrical shorts, as a result of solder bridges, if they are subjected to reflow. There are two popular methods for package alignment using machine vision:

Package silhouette The vision system locates the package outline. Terminal recognition Some vision systems can directly locate on the pad metallization pattern.

Both methods are acceptable for  $\mu$ Module placement. The terminal recognition type alignment tends to be more accurate, but is also slower since more complex vision processing is required of the pick and place machine. The package silhouette method allows the pick and place system to run faster, but is generally less accurate. Both methods are acceptable, and have been successfully demonstrated by major pick and place equipment vendors and contract PCB assembly houses.

#### 5.2 Solder Reflow

µModules, which are shipped in moisture barrier bags, require special handling to insure proper surface mount conditions are met. The moisture barrier bag will be labeled with the proper instructions concerning the correct handling of the uModules. uModules exposed to room temperature and humidity conditions beyond the cumulative time specified on the label must be baked prior to surface mount. Module size and weight determine the bake conditions and bake times. Industry standard bodies such as JEDEC publish tables with bake times and temperatures. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile should be checked at different locations on the board. Component temperatures may vary because of surrounding components, location of the device on the board, and package densities. To maximize the self-alignment effect of a  $\mu$ Module (see Figure 3), it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded. A good guide is to subject the PCB to a temperature ramp not exceeding 4°C per second. The reflow profile guidelines are based on the temperature at the actual solder pad to PCB land pad solder joint location. The actual

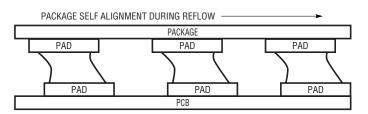


Figure 3. Solder Mask Not Shown For Clarity (Not To Scale)

temperature at the solder joint is often different than the temperature settings in the reflow/rework system due to the location of the system thermocouple placement used to monitor the temperature. The furnace needs to be profiled using thermocouples at various locations on the PC board. A thermocouple should be placed on one of the largest and smallest components on the PCB. It is suggested that the peak temperature differential between the smallest and largest package be 10°C or less for average size PC boards. Reference Jedec/IPC Standard J-STD-20b for reflow recommendations. µModules are typically moisture sensitive and fall into level classifications defined by JEDEC. Specific levels are stated on moisture sensitive labels shipped with LTC devices. All LTM µModules are lead free and Linear Technology has tested the µModules for a specific reflow profile (245°C peak body temperature).

An example of a specific board mount lead free profile for an LTM4600 module is discussed. The module was mounted on a 0.06in thick, 3in × 3.75in, 4-layer FR4 board using a lead free solder paste. Thermocouples were placed on the module LGA pads and on the bottom of the FR4 board to monitor the temperatures at these locations. A third thermocouple to monitor the oven environment temperature was also attached on top of the FR4 board. The temperature profile was monitored on seven different oven zones at approximately 30 seconds apart. The data gathered and the temperature profile used to mount the LTM4600 module to this board is shown in Table 2, Table 3 and Figure 4. To achieve this profile, the oven environment was set to 260°C maximum with a maximum zone slope of 2.0°C /sec. From Table 2, it is important to note that the LTM module only achieves a maximum temperature of 243°C even though the oven temperature is set to 260°C. This is consistent with LTC reflow requirement of 250°C maximum for the LTM4600 module body temperature. Analyses of the solder joint obtained from this profile indicate excellent joint formation.

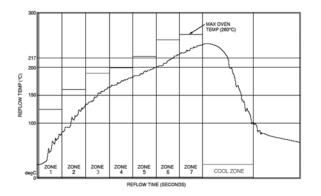


	TEMP (°C)		TIME (SEC.)				
	MIN	MAX	150°C to 217°C	217°C to 243°C	At 243°C		
LGA (Under)	24	243	99	72	15		
Board (Top)	26	249	105	74	15		
Board (Under)	26	244	105	68	15		

#### Table 2. LTM4600 Module Reflow Profile Parameters

#### Table 3. LTM4600 Module Reflow Profile Parameters

	ZONE SLOPES (°C/Sec)							
	1	2	3	4	5	6	7	Cool Down
LGA (Under)	2.0	1.3	0.8	0.6	0.6	0.8	0.3	-2.4
Board (Top)	2.3	1.6	0.7	0.5	0.6	0.8	0.4	-2.6
Board (Under)	2.1	1.6	0.7	0.5	0.6	0.8	0.4	-2.3



#### Figure 4. Temperature Reflow Profile for an LTM4600 Module

#### **5.3 PCB Cleaning**

Residue from the surface mount process can create resistive connections between pads on LGA packages. If a low residue, no-clean solder paste is used, PCB cleaning is not required and has little effect on a  $\mu$ Module. With the elimination of materials containing CFCs, most companies have moved to a no-clean or aqueous flux-based system. "No clean" fluxes and solders simply mean that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board. Residues have sometimes been shown to be a collection point for outside contamination on the board surface. Because there are so many different types of no-clean solder pastes available, application specific evaluations should be performed to identify if any remaining residue still needs to be removed from the boards in final production.

#### 5.4 Inspection

Inspection of a µModule on a PCB is typically accomplished by using transmission type X-ray equipment. In most cases, 100 percent inspection is not performed. Typically X-ray inspection is used to establish process parameters, and then to monitor the production equipment and process. Transmission X-ray can detect bridging, shorts, opens and solder voids. There are many different types of X-ray inspection equipment available and functionality varies. X-ray inspection system features range from manual to automated optical inspection (AOI). Different systems also provide single or multiple dimensional inspection capabilities.

As explained in section 5.1 of this guide, a  $\mu$ Module will self align to the land pad using surface tension during the solder reflow process. As a result, it is unlikely that a  $\mu$ Module will be marginally misaligned. If misalignment does occur it is likely to be by an entire pad. This effect makes it possible to do a gross visual alignment check after reflow. Visual checks can be aided by the use of PCB fiducial marks which also aid manual placement of units during any rework.

#### 6.0 Rework

 $\mu$ Module rework procedures are an adaptation (and in some cases a simplification) of Ball Grid Array Package rework procedures. The basic elements of this procedure are as follows:

- PC board bake 125°C for 24 hours
- PC board preheat 125°C
- · Reflow of component solder
- Vacuum removal of component
- Cleaning and prep of PCB lands
- Screening of solder paste
- Placement and reflow of new component
- Inspection of solder joints



#### 6.1 PC Board Bake

It is recommended to bake the PCB for approximately 24 hours at 125°C prior to rework in order to drive off residual moisture that could cause other component failures during the rework reflow process.

#### 6.2 PC Board Preheat

Once the PCB has finished the baking process, the PCB under rework is then placed in the rework holder and preheated to a temperature of 125°C. Localized heating of the area under rework is recommended. (Use 4°C/second maximum ramp rate)

#### 6.3 Reflow/Removal of the Component from the PCB

Specialized vacuum collets come in contact with the rework component. These collets incorporate a hot gas shroud that heats up the part to a temperature required for reflowing the solder interconnects. Once the solder reflows, the vacuum collet lifts the unit from the PCB. The collet size and hot gas flow should be optimized to keep the heat flow localized to the component being removed, while uniformly heating the component.

#### 6.4 Cleaning and Prep of the PCB Land

The PCB can be cleaned and prepared using conventional tools and processes currently used for gullwing packages. Removal of excess solder using a hot iron, a small scraping tool and solder wick is typical. Place the solder wick under the scraping mechanism to remove the solder from the land area.

#### 6.5 Screen Printing of Solder Paste

Based on some of the tight geometries used on today's PCBs, it is difficult to screen print a PCB that is nearly 100% populated with components. Hence the approach of

manual screen-printing the solder paste directly onto the new component has been adopted. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in this application note.

#### 6.6 Placement and Reflow of Component

The placement of the new  $\mu$ Module component should be done with a split field vision system. The image of the screen-printed component and the PCB land pattern are superimposed during the placement operation, thus making the placement easier to align with the terminal footprint.

The reflow of the new component should be done with a localized gas shroud similar to that used during the component removal operation. The profile used for the reflow should have ramp rates and peak temperatures that follow the guidelines specified in this outline.

#### 6.7 Inspection of Reworked Solder Joints

Inspection techniques for the  $\mu$ Module closely resemble those techniques used for Ball Grid. Array components. Visual inspection of solder joints from overhead (z-plane) is not possible for these packages. Thus, the use of z-plane X-ray or a high precision camera system capable of viewing parallel to the x-y plane is necessary.

#### 6.8 Rework Equipment for $\mu \text{Module}$

Rework systems for the  $\mu Module$  are based on well-established rework systems created for Ball Grid Array packages.

#### **7.0 MATERIALS DECLARATION**

Materials declarations can be obtained through Linear Technology. Please contact your local representative.

#### APPENDIX A

#### PRODUCTION PRINT STENCIL DESIGN GUIDELINES FOR THE INTEGRATED POWER $\mu\text{MODULE}$

James R. Staley

The DC/DC  $\mu$ Module provides high density power in a small 15 mm  $\times$  15 mm package, reducing circuit area and design time. These advantages, however, are contingent upon the device being reliably coupled to the circuit board to ensure rated performance and to reduce the possibility of circuit failure. Currently, the most effective method for mounting the module to the circuit board during production assembly involves printing solder paste to the circuit board through the use of a stencil. The stencil must be designed carefully to accurately reproduce the desired print design through the efficient release of the solder paste, yet be rugged enough to withstand the stress of repeated flexing and scraping imparted by the squeeze blade during the print process. The goal of this article is to give the reader a distilled treatise on the aggregate considerations of stencil design that apply to the  $\mu$ Module.

Stencils offer a convenient way of placing solder paste in a controlled and repeatable manner upon the circuit board, yet much care must be taken when designing them. Every dimension is usually critically interdependent with other dimensions and involves a number of compromises that act to hinder the print accuracy and consistency. **The goal of the stencil designer is to create an ideal pattern that places the same volume of solder on every identical feature on each board time after time.** While this is never fully achieved, careful attention to the details in this article will place the actual results obtained closer to the ideal goals.

The stencil must be durable enough to withstand the repeated stresses involved in the printing process. A laser cut stainless steel stencil works best for printing the module grid array. The laser produces sharp edges, smooth inside areas with a slight taper that aids in the separation, increasing release efficiency. The stencil should be oriented during production such that the wider aperture opens to the circuit board (for production stencils) or against the device (for re-work stencils). This is usually the side facing the laser. The narrower aperture should always be the paste application side.

Stencil thickness is a critical factor when designing the aperture dimensions. The practical limit, even with 100% paste deposition, in stencil thickness becomes the dot (individual lump of printed paste) volume. For the µModule and similar applications, the stencil should be kept between 0.004" to 0.006" (0.1mm to 0.15mm) for volumetric constraints. Using thicker stencils may increase the probability of balling and bridging, while compensating for the increased thickness with a reduction in aperture size diminishes the release efficiency, leading to less predictable deposition and dot volume, resulting in open joints. Using thinner stencils necessitates the use of a 1:1 aperture to feature ratio which increases the chances of even minor misalignment causing balling, while any reduction in the aperture to feature ratio or less than perfect release threatens insufficient volume, starved or open joints, and may lead to poor mechanical strength.

Regardless of the stencil features, proper care must be given to the printing process at the factory and are best handled by qualified technical staff at the fabrication site. The preparation, paste rheology, handling time, standoff distance, blade hardness and speed, and re-flow process details are critical in conjunction with careful stencil design to ensure maximum yield and minimum failure rates. It is important to find out what printing techniques are used at any assembly house or factory where the  $\mu$ Module will be installed. Each of these sites should be able to provide recommendations for stencil design limitations.

The following aperture dimensions provide a good starting point for design, and are based on the common stencil stock at 0.004", 0.005" and 0.006" thickness (see Figure A1). As with any reference, it remains the PCB designer's responsibility to verify the proper and reliable operation of the stencil in the actual application. Variation from the recommended dimensions may significantly affect printing performance or reliability.



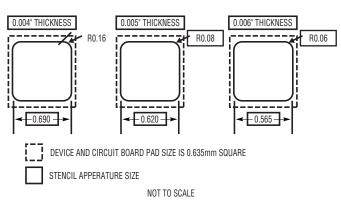


Figure A1. Recommended Aperture Dimensions For Commonly Used Stencil Material Thickness

There are several important considerations to consider when designing a production or re-work stencil. Since the aspect ratio of the stencil is quite high given the relatively large aperture size of the  $\mu$ Module contacts, these considerations are not nearly as critical as when designing for fine pitched peripheral-array parts such as found on Linear Technology parts in QFN and DFN packages. The  $\mu$ Module features a BGA-like contact design with no exposed heel due to the use of a laminate, and for this reason the production and rework stencil artwork will be identical. A typical rework stencil is slightly larger than the part itself, measuring less than a few inches across square, and having a mechanical block with a cut-out held to tight dimensions adhered to it to center the part and provide mechanical rigidity.

The aperture dimensions in Figure A1 have been sized to keep the average dot volume near 0.04mm<sup>3</sup>, which will provide an adequate amount of solder to assure that all contacts have an optimum balance between electrical and

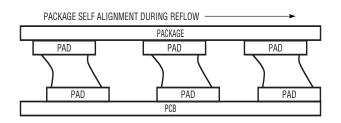


Figure A3. Poorly Designed Apertures Jeopardize Release Efficiency and Result in Inconsistent Dot Volume

mechanical performance with a typical standoff distance of  $38\mu$ m (1.5mils) (see Figure A2). To this end, it is recommended to use non-solder mask defined land features on circuit boards incorporating  $\mu$ Module products. This will provide the planar contact grid additional robustness for withstanding mechanical stress and aid in conductance and thermal transfer.

Extensive testing has shown that for laser-cut stencil use, transfer efficiency depends greatly on the area ratio of artwork apertures, especially as the pitch increases. For the  $\mu$ Module, the feature size is nominally large, so release efficiency will depend more heavily on factors outside of the stencil designer's control, such as paste rheology, blade pressure, and especially separation speed. Still, it is worth noting that the recommended apertures shown have a trend of decreased area ratio as the stencil thickness increases. In general, laser-cut stencils should be designed with a minimum area ratio of 0.66, and at this low value extreme, transfer efficiency will likely suffer.

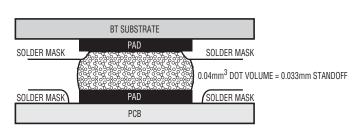
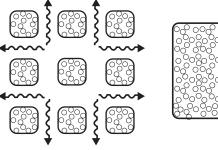


Figure A2. Good Mounting Depends on Standoff and Bump Volume







Aperture reduction is employed to prevent paste from contacting solder mask under any circumstances, thereby preventing balling or bridging. Since perfect alignment is never a practical expectation, some margin must be left to account for stencil to PCB alignment during printing and device to PCB alignment during placement (Figure A3). This is accomplished by undersizing the aperture from the land pattern by a recommended dimension of 0.025mm from all edges. Note that this is not possible when using 0.004" stencil thickness, or dot volume suffers. A good compromise is the 0.01mm recommendation as shown, which should provide adequate margin for placement offset, yet also keeps the dot volume very near 0.04mm<sup>3</sup> as shown in Figure A4.

The contact array utilized by the  $\mu$ Module provides the additional benefit of having a web of channels for outgassing to occur without danger of splatter or bridging as shown in Figure A4. This eliminates the necessary calculations and design compromises necessary when designing stencils where artwork includes a large open contact area, such as the QFN and DFN packages.

Bearing these details in mind and using the recommended dimensions as a starting point, stencil design for the  $\mu$ Module power module should not be complicated nor store any hidden pitfalls often encountered with fine pitch parts. The importance of a well-designed stencil is realized in a high assembly yield and no field failures caused by problems whose origin lay in assembly defects due to poor joints brought on by inconsistent dot placement.

#### References

1. Coleman, William E: Stencil technology and stencil design guidelines for print performance. Photo stencil, Colorado Springs, CO.

2. IPC-7525: Stencil design guidelines. ISBNI±1-580982-45-x. May, 2000.

3. Primavera, Anthony A: Influence of PCB parameters on chip scale package assembly and reliability. Surface Mount Technology Laboratory, Universal Instruments Corporation. Binghamton, NY.

4. Dr. Huang, Benlih and Dr. Lee: Solder bumping via paste reflow for area array packages. Indium Corporation of America. Utica, NY.

5. Koki Company Ltd: General information on solder paste. Online PDF publication from Koki Company distributor website.

6. Skyworks Application Note: PCB Design and SMT Assembly/Rework – Guidelines for MCM-L Packages. Document 101752C July, 2002.

7. Conexant Application Note: MCM-L Package Types – Integration into PWB Designs. Document 101049A June, 2000.

8. Amkor Technology Application Note: Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages. March, 2001.

